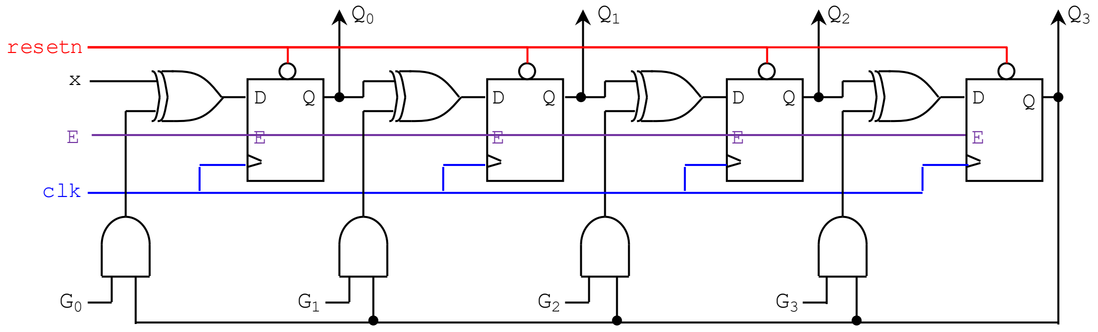
Homework 4

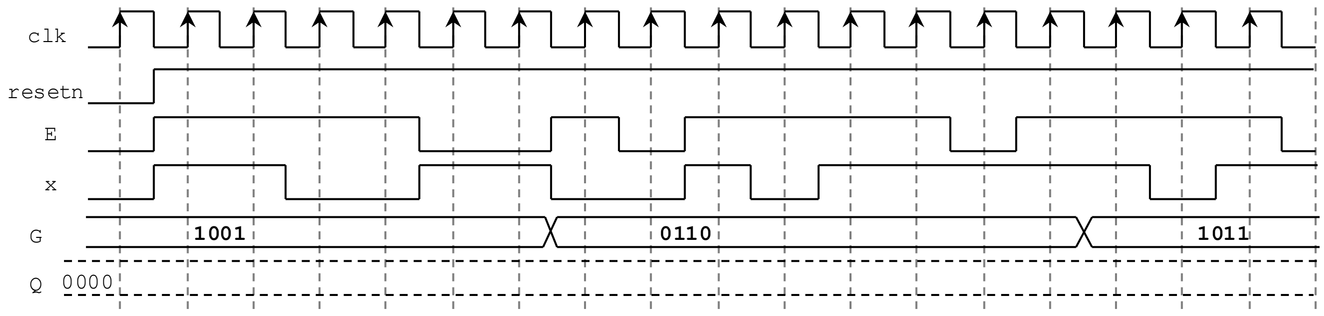
(Due date: November 21st @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (14 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0$, $Q = Q_3Q_2Q_1Q_0$.



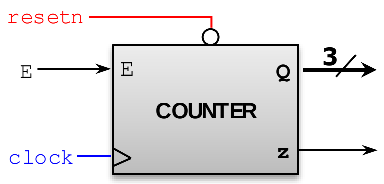


PROBLEM 2 (18 PTS)

Design a counter using a Finite State Machine (FSM):

Counter features:

- ✓ Count: **000**, 010, 111, 011, 110, 100, 001, 101, **000**, 010, 111, …
- ✓ $resetn$: Asynchronous active-low input signal. It initializes the count to "000"
- ✓ Input E: Synchronous input that increases the count when it is set to '1'.
- ✓ output z: It becomes '1' when the count is 101.

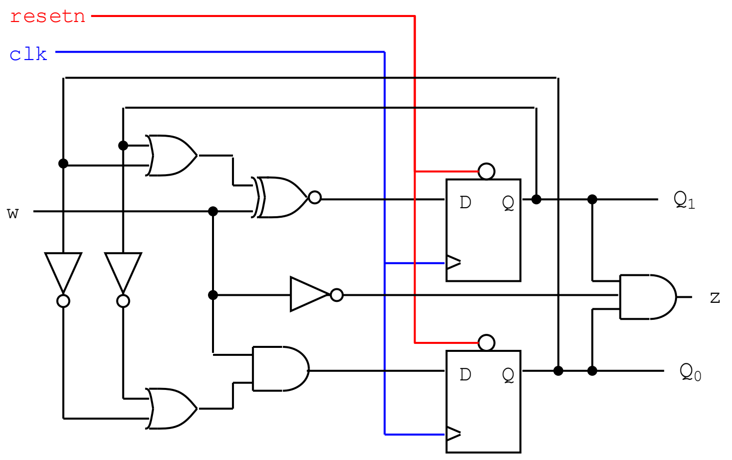


- Provide the State Diagram (any representation), State Table, and the Excitation Table. Is this a Mealy or a Moore machine? Why? (10 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

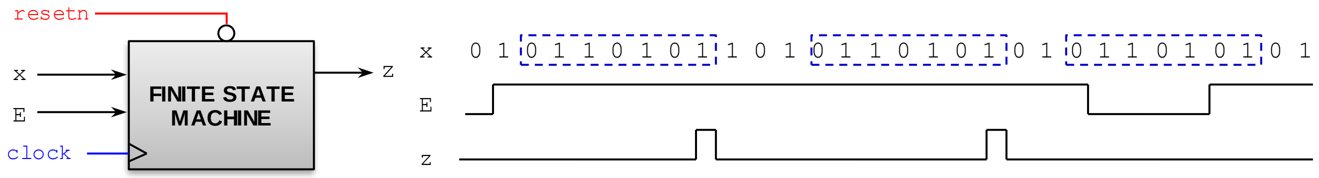
PROBLEM 3 (20 PTS)

- Given the following State Machine Diagram. (10 pts).
  - ✓ Provide the State Diagram (any representation) and the Excitation Table,
  - ✓ Provide the Excitation equations and the Boolean equation for z.

  w: input, z: output, Q_1Q_0: state.



- **Sequence detector**: Provide the State Diagram (any representation) and the Excitation Table of a circuit with inputs x and E and output z. The machine has to generate $z = 1$ when it detects the sequence 0110101. Right after the sequence is detected, the circuit looks for a new sequence. (10 pts).
  The signal E is an input enable: It validates the input x, i.e., if $E = 1$, x is valid, otherwise x is not valid.

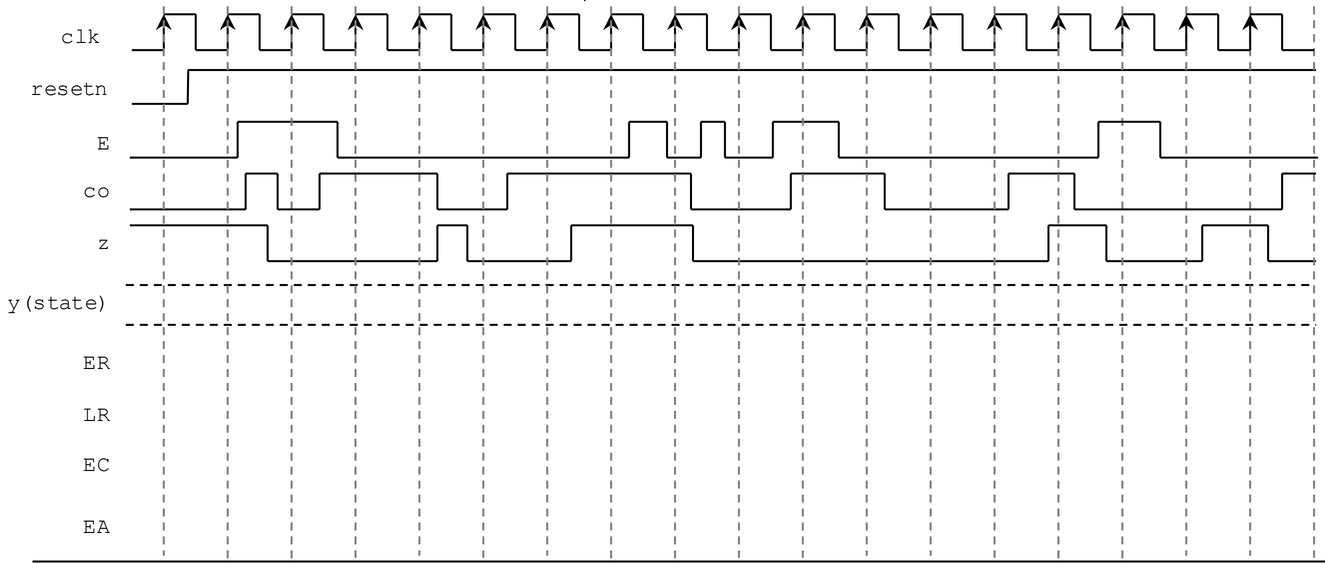


PROBLEM 4 (15 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

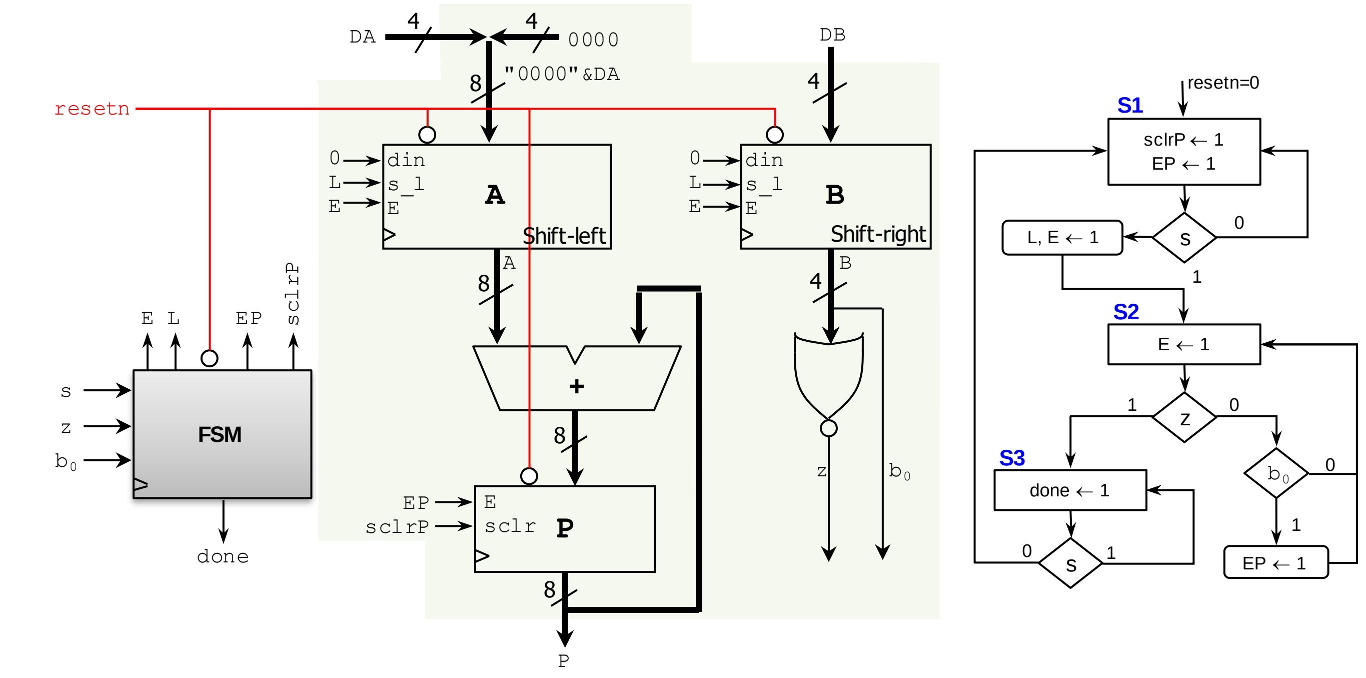
```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, resetn: in std_logic;
          z, E, co: in std_logic;
          ER,LR,EC,EA: out std_logic);
end myfsm;
```

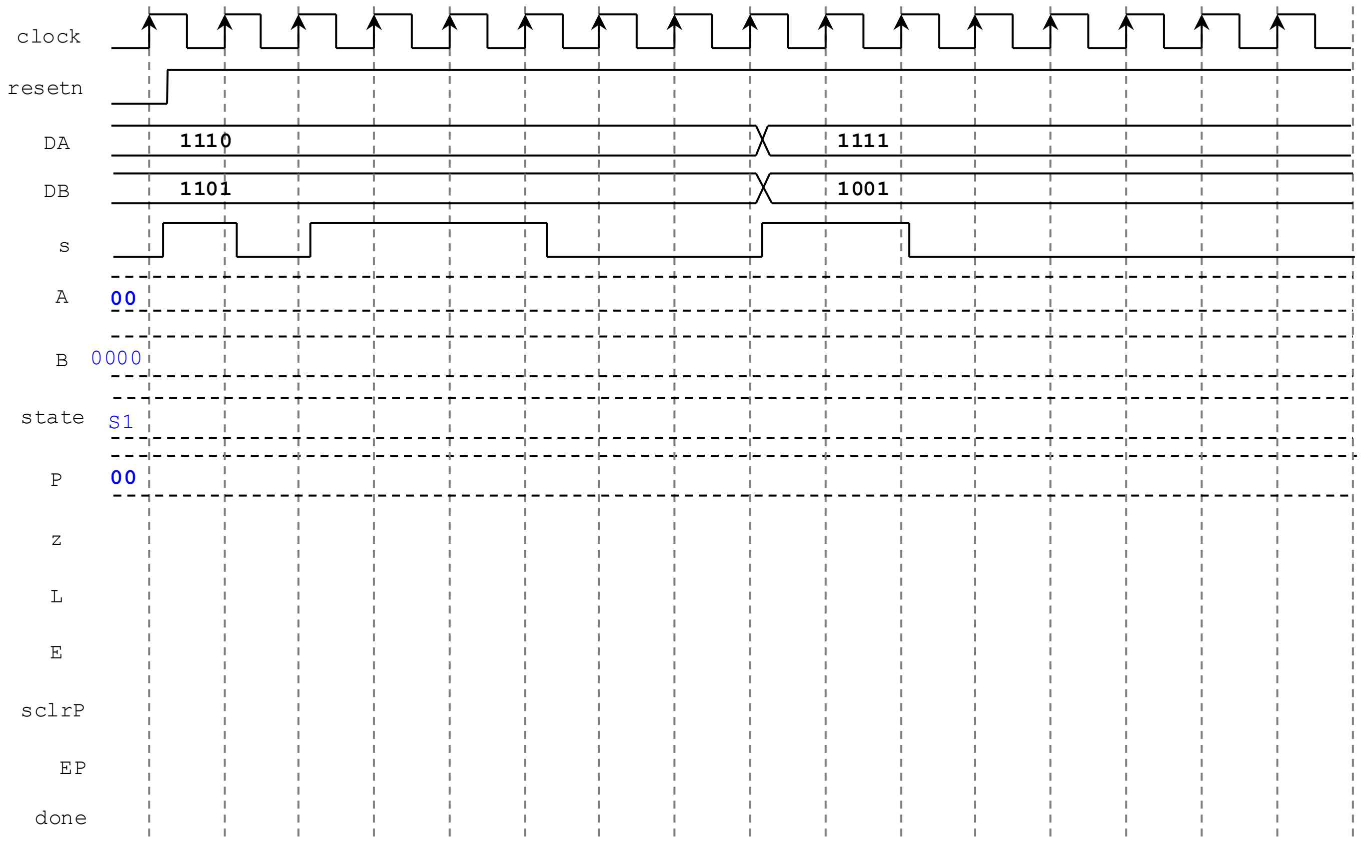
```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, z, E, co)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if E = '1' then y <= S2; else y <= S1; end if;

          when S2 =>
            if z = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if E = '1' then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, z, E, co)
  begin
      ER <= '0'; LR <= '0'; EC <= '0'; EA <= '0';
      case y is
         when S1 => ER <= '1'; EC <= '1';
                    if E = '1' then EA <= '1'; end if;

         when S2 => ER <= '1'; EA <= '1';
                    if co = '1' then LR <= '1'; end if;
                    if z = '0' then EC <= '1'; end if;

         when S3 =>
      end case;
  end process;
end behavioral;
```



PROBLEM 5 (18 PTS)

- Complete the following timing diagram (A and P are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
Register (for P): $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
Parallel access shift registers (for A and B): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift





PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (one or two pages). This report should contain the current status of the project, including a block diagram of your system. You **MUST** use the provided template (`Final Project - Report Template.docx`).